REMARKS

Claim 5 is cancelled without prejudice and the limitations included in amended claim 1. Claim 27 is cancelled without prejudice and the limitations included in amended claim 25. The amendments are made for the purpose of expediting prosecution and not for patentability, and the claim cancellations are made without prejudice. Applicant reserves the right to pursue subject matter of the original claims (prior to amendment) and subject matter of the cancelled claims in subsequent prosecution. Claims 1-4, 6-26, and 28-39 remain for consideration. All claims are thought to be allowable over the cited art.

The Office Action does not establish that claims 1-39 are anticipated under 35 U.S.C. §102(e) by "Charlton" (US Patent 6,289,292 to Charlton et al.). The rejection is respectfully traversed because the Office Action does not show that Charlton teaches all the limitations of the claims.

Claims 1 and 25 are amended to include limitations of and related to implementing the user design in a defective PLD. As explained below for claims 9 and 33, the Office Action does not show that Charlton teaches these limitations.

In regards to claims 9 and 33, the Office Action fails to show that Charlton teaches the limitations of "implementing the user design in the first defective PLD ...". As to the limitations of the "design" being implemented, the Office Action apparently construes the corresponding "design" from Charlton to be memory module 10 of Charlton's FIG. 5. However, if this is the teaching that allegedly corresponds to the limitations of and related to "implementing the user design," then the claim limitations are not taught by Charlton. The claim limitations clearly indicate that the design is implemented in a defective PLD. The cited portion of Charlton apparently teaches that the design includes defective memories. The cited teachings of Charlton do not teach implementing any design in a PLD or even in the defective memories. Rather, the defective memories are part of the design. Therefore, the Office Action fails to show that Charlton teaches all the limitations of claims 9 and 33.

The Office Action fails to show that Charlton teaches all the limitations of independent claim 20. Claim 20 includes limitations of performing an incremental

compilation with respect to the first design file while using the first location information to avoid the localized defects of the first defective PLD, the incremental compilation generating a second design file; and providing the second design file to the user. The Office Action does not appear to allege any teachings of Charlton as corresponding to these limitations, and these limitations do not appear to be taught by Charlton. Therefore, claim 20 is not shown to be anticipated by Charlton.

Claims 2, 10, 21, 26, and 34 depend from claims that, as explained above, are not shown to be anticipated by Charlton. Therefore, the Office Action fails to show that these claims are anticipated by Charlton.

Claims 3 and 11 include limitations of the location information including identification information for at least a portion of one or more logic blocks affected by the localized defects. It is respectfully submitted that the none of the cited teachings of Charlton suggest the limitations related to a PLD. Therefore, Charlton is not shown to suggest that the location information includes identification information for logic blocks of a PLD, and claims 3 and 11 are not shown to be anticipated.

Claims 4 and 12 depend from claims that are not shown to be anticipated. Therefore, the Office Action does not establish that claims 4 and 12 are anticipated.

Claims 5 and 27 (both now cancelled) are not shown to be anticipated by Charlton for at least the reasons set forth above for claims 9 and 33.

Claim 13 includes limitations of performing an incremental compilation with respect to the first implemented design as part of implementing the user design in the first defective PLD. It is respectfully submitted that there is no apparent teaching by Charlton of incremental compilation. Nor does the Office Action cite any particular teaching as corresponding to these limitations. Therefore, claim 13 is not shown to be anticipated.

Claims 6, 28, and 35 depend from claims that are not shown to be anticipated, and therefore, the Office Action does not establish that Charlton anticipates these claims.

Claims 7, 16, 23, 29, and 36 includes limitations of the PLD being a field programmable gate array (FPGA), and the Office Action cites Charlton's teachings of testing of devices including, but not limited to memory such as PROMs and EPROMs.

However, these cited examples are both memory devices. Further, an open statement by itself does not suggest the specific claim limitations of and related to an FPGA. Therefore, these claims are not shown to be anticipated by Charlton.

Claims 8, 17, and 24 include limitations of and related to a constraints file. It is respectfully submitted that those skilled in the will recognize that a constraints file specifies logic blocks or portions thereof in which implementation software may not place user logic (paragraph [0020]). Charlton is cited as generally teaching describing defect locations. However, there is no apparent teaching or suggestion of the specific use of a constraints file as claimed. Therefore, claims 8, 17, and 24 are not shown tot be anticipated by Charlton.

Claim 14 depends from claim 9 and is not shown to be anticipated for at least the reasons set forth above.

Claim 15 depends from claim 14 and includes further limitations of performing an incremental compilation with respect to the first implemented design. As explained above in regards to claim 13, Charlton is not shown to teach or suggest incremental compilation. Thus, the Office Action does not show that claim 15 is anticipated.

Claim 18 includes limitations of the defective PLD being an FPGA that is programmable from a PROM, and implementing the design in the defective PLD by PROM programming software. These limitations are clearly not shown by the Office Action to be taught by Charlton. The cited teachings of Charlton appear to merely suggest that a PROM may be tested and the defects are mapped. There is no apparent suggestion that a defective FPGA may be programmed from a PROM as claimed. Therefore, claim 18 is not shown to be anticipated.

Claim 19 depends from claim 16 and includes further limitations of placing and routing the user design in the first defective PLD while using the location information to avoid using defective portions of the first defective PLD; and generating an FPGA bitstream implementing the user design in the first defective PLD. As explained above, Charlton is not shown to suggest any application to a PLD. Furthermore, there is no apparent teaching of placing and routing a design, nor is there any apparent teaching of generating an FPGA bitstream as claimed. The cited portions of Charlton map bit errors in memory devices and determines characterization values. Thus, there

is no apparent correspondence to placing and routing nor to generating an FPGA bitstream. Therefore, the Office Action does not establish that claim 19 is anticipated.

Claim 22 depends from claim 20 and includes further limitations of incremental compilation as discussed above for claim 20. Thus, for at least the reasons set forth above claim 22 is not shown to be anticipated by Charlton.

Claim 30 depends from claim 25 and includes further limitations of the device-specific information including information relating to the speed of various sub-components of the PLD. From claim 25, a PLD is tested for the device-specific information. There is no apparent suggestion by Charlton of speeds of components of a PLD being used as the device-specific information. Furthermore, the cited teachings relate to bit defect information and a characterization value. There is no apparent relevance of Charlton's bit defect information to the claimed speeds of sub-components. Thus, claim 30 is not shown to be anticipated by Charlton.

Claim 31 depends from claim 25 and includes further limitations of the device-specific information being configuration information for the PLD. The Office Action fails to show that these limitations are taught by Charlton. As with claim 30, the Office Action cites Charlton's teachings of bit defects and use of a characterization value as corresponding to these limitations. However, those skilled in the art will recognize that configuration information for a PLD is not suggested by bit defects of a memory device. Thus, claim 31 is not shown to be anticipated.

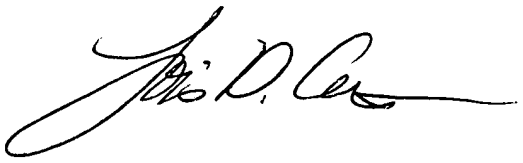
Claim 32 depends from claim 25 and is not shown to be anticipated for at least the reasons set forth above for claim 25.

Claims 37, 38, and 39 depend from claim 33 and set forth limitations comparable to the limitations of claims 30-32. Therefore, the Office Action fails to establish that claims 37-39 are anticipated by Charlton.

CONCLUSION

The Office Action fails to establish that the pending claims are anticipated in view of the cited reference. Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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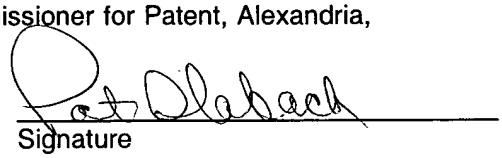
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